Application No. **09/731,889**

LED chip packaging w/layered electrodes

East Search

1/30/02

Search	L No.	Hits	Text Search			Data Bases
IS&R	L2	3254	("257/784,775,736,748,750,762,766").CCLS.		1/30/02 9:53	USPAT; EPO; JPO; Derwent; IBM TDB
BRS	L7	1063	2 and (AU cu ni)		1/30/02 10:38	USPAT; EPO; JPO; Derwent; IBM TDB
BRS	L9	35	7 and bond adj pad		1/30/02 10:04	USPAT; EPO; JPO; Derwent; IBM TDB

Search Result

USPAT	Date	Page	Title	Cl/Sub	Cl/Sub	Inventor
US 6300687 B1	20011009	18	Micro-flex technology in semiconductor packages	257/784	257/686	Bertin, Claude Louis , et al.
US 6169330 B1	20010102	9	Method and apparatus for packaging high temperature solid state electronic devices	257/782	257/677 ; 257/697 ; 257/703 ; 257/781 ; 257/784 ; 438/612 ; 438/613 ; 438/615 ; 438/617	Pankove, Jacques Isaac
US 5495667 A	19960305	11	Method for forming contact pins for semiconductor dice and interconnects	29/843	174/260 ; 228/155 ; 257/780 ; 257/784 ; 438/117	Farnworth, Warren M. , et al.
US 5298793 A	19940329	4	Semiconductor device including an electrode	257/765	257/766 ; 257/771 ; 257/784	Kotani, Jutaro , et al.
US 5227662 A	19930713	10	Composite lead frame and semiconductor device using the same	257/676	257/666 ; 257/668 ; 257/675 ; 257/784	Ohno, Yasuhide , et al.